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RAPID COMMUNICATION

Micropower thermoelectric generator from thin Si membranes

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Abstract
We report the development of a Si-based micro thermogenerator build from silicon-on-insulator by using standard CMOS processing. Ultrathin single-crystalline Si membranes, 100 nm in thickness, with embedded n and p-type doped regions electrically connected in series and thermally in parallel, are active elements of the thermoelectric device that generate thermopower under various thermal gradients. This proof-of-concept device produces an output power density of 4.5 $\mu W/cm^2$, under a temperature difference of 5 K, opening the way to envisage integration as wearable thermoelectrics for body energy scavenging.

Introduction

The potential decrease of fossil fuel supplies and the urgent need to reduce green-house gas emissions drives mankind into the necessity to search for alternative, greener, sources of energy. Among the various available energy sources, waste-heat energy is universally present since any heat engine, from biological entities at nearly room temperature to high-temperature combustion processes, will dissipate part of its energy in the form of heat. An efficient conversion of this excess heat into useful forms of energy, i.e. electricity, remains a challenge and it is the subject of intense investigation [1–4]. In this respect, thermoelectric materials that convert heat differences across the material into electricity could help meeting the energy challenge of the future. The efficiency of this energy conversion relies on the capacity of the material to transport electrical charges while impeding the flow of heat. A useful indicator of the goodness of a TE material is the

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Nomenclature

I	current, A
P	thermoelectrical power, W
R_{int}	internal resistance, Ω
R_{load}	load resistance, Ω
S	Seebeck coefficient, V/K
T	temperature, K
$V_{seebeck}$	Seebeck voltage, V
V_{oc}	Seebeck voltage in open circuit, V
ZT	thermoelectrical figure-of-merit, $ZT=(S^2\sigma/\kappa)T$

Greek

κ	thermal conductivity, W/mK
σ	electrical conductivity, S

Abbreviations

CMOS	complementary metal oxide semiconductor
FEM	finite element modelling
LPCVD	low pressure chemical vapor deposition
NW	nanowire
PDEs	partial differential equations
RIE	reactive ion etching
RTA	rapid thermal annealing
SOI	silicon on insulator
TE	thermoelectric/al
TEG	thermoelectric/al generator
TMAH	tetramethylammonium hydroxide

Figure-of-Merit, ZT, an adimensional parameter that relates the Seebeck coefficient, S, the electrical conductivity, σ, and the thermal conductivity, κ, at a given temperature, as $ZT=(S^2\sigma/\kappa)\times T$. A material with large ZT can be termed a phonon glass-electron crystal, but unfortunately, no material in nature fulfills these requirements to the desired level. Currently, heavy semiconductors of the BiSbTe family with consistent values of ZT up to 1.5 are the best thermoelectric materials at medium-to-low temperatures [5,6]. However, Bi(Sb)Te, already used in commercial Peltier devices, lacks proper integration with standard CMOS processing. Although the main motivation of introducing TE devices in the computer industry was to replace forced-air to cool microelectronics integrated circuits systems, new "niches" of application appears such as temperature stabilization in optoelectronics devices and power generation of portable and wearable micropower applications. Therefore, integration of these materials into chip-harvesting devices is necessary, while technically challenging. Doped bulk-Si may appear as an appealing alternative but its figure-of-merit is remarkably low, $ZT=0.01$ at 300 K, precluding its use in any of the proposed applications. Actually, poly-silicon thermogenerators, formed by many elements per device, have already been fabricated in an augmented BiCMOS process [7,8], however their low power output limits the range of applications. Nanostructuration has been presented as a convenient route to improve the figure of merit [9] and a recent breakthrough has challenged the view that Si is a poor thermoelectric [10,11]. It was shown that Si nanowires (NW) exhibit a figure of merit enhanced by 100× compared to their bulk counterpart. This remarkable behavior is mainly due to the reduction of the thermal conductivity associated to phonon scattering with the boundaries of the NW, while preserving bulk values for the electrical conductivity and the Seebeck coefficient. Although still insufficient for many applications that require ZT in excess of 3, this finding opens the use of low-dimensional Si as a thermoelectric material in miniaturized chips that can be monolithically integrated into CMOS-compatible devices for low-power applications. There are already several examples that employ low-dimensional Si obtained from bottom-up or top-down approaches in planar or vertical geometries [12-14]. The most extended device structure has a vertical configuration (column type) with the n-p legs connected thermally in parallel and electrically in series. Several vertical n-p type thermo-electrical generators (TEG), using top-down synthesized Si NWs, were recently fabricated and tested [12,13]. The output power in the device fabricated by Li et al. was limited to few μW per

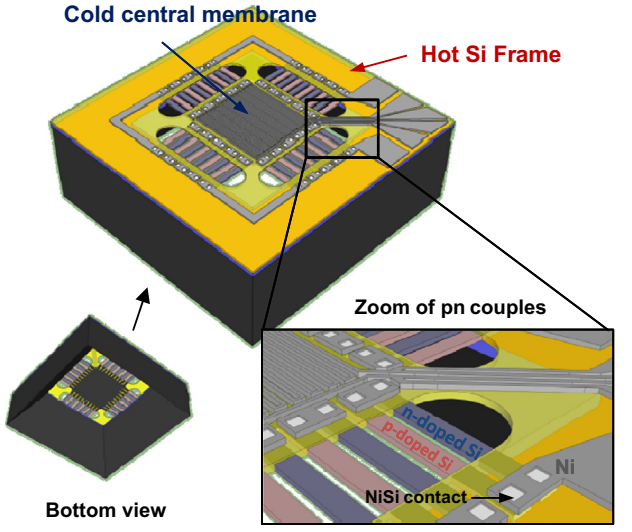

Figure 1 Schematics of the device. Main Draw: gray color show the Ni metal lines, yellow the silicon nitride layer. In this version of the device the central region is filled with a metal for heating/sensing purposes. Better observed in the zoom view, red and blue regions represent the n, p couples defined in the Si membranes and white the NiSi intermetallic at the open via contacts. Bottom view: shows the free standing membrane after back side Si bulk etching.

device due to the reduced ΔT=0.12 K achieved across the 1 μm Si NWs [12]. A power output of 29.3 μW with ΔT of 56 K for a 50 μm × 50 μm device was achieved by Bowers and coworkers in a unileg device using a highly ordered Si nanowire array composite [13]. A planar device also based on Si NWs grown by the VLS method at high temperature was fabricated by Davila et al. [14]. This unileg device has a high density of NWs with a total distance between the hot and cold regions up to 90 μm. Power outputs of 9 μW/cm^2 and 1.4 mW/cm^2 were achieved under temperature differences of 27 and 300 K across the device, respectively.

Alternatively, thin films can also be used to build a thermoelectric generator [6,15]. In this case the vertical geometry is sometimes not adequate since the temperature of the cold side increases rapidly by heat conduction and radiation from the hot side. A planar configuration with horizontal gradients has been shown to be more effective for a thin film TEG since the heat flow is parallel to the thin film and larger ΔT can be achieved [15]. Furthermore, reduction of film thickness to the nm range will increase phonon scattering with the boundaries compared to bulk materials, enabling higher temperature differences and therefore higher power outputs.

Bottom-up approaches to fabricate the desired nanostructured material integrated in the chip-harvesting module often lack enough reproducibility to guarantee the required fabrication yield. Therefore, we propose a top-down strategy in combination with a planar configuration to fabricate a TEG device that uses low-dimensional Si as the main thermoelectric material. In this article we detail the fabrication procedure and the critical steps towards obtaining a reliable and efficient TEG comprising n and p-type legs made from an ultrathin Si suspended membrane. We model the thermoelectrical behavior of the device and measure the power output at various ΔT by measuring IV curves under different loads.

Material and methods

Device design and microfabrication procedure

The design of the TEG is shown in Figure 1. It consists of a planar device with a suspended very thin Si platform at the center (500 × 500 μm^2) contacted to a Si frame through ultrathin n and p-type Si membranes, 50 μm wide × 150 μm long. The distance between hot and cold regions is also approximately 100 μm. In this particular design, 20 np couples are distributed along the 4 sides of the central platform.

We start the microfabrication process (See Figure 2) with a Silicon on Insulator, SOI, wafer with a 340 nm Si device and 400 nm buried oxide layers. The upper Si layer is reduced to 100 nm by wet oxidation and subsequent HF etching. This layer is patterned and etched (RIE) until the buried oxide is reached, to create a central squared silicon region of 500 μm × 500 μm (undoped region) and 50 μm × 150 μm "legs" surrounding it (doped n,p regions). A thin, 50 nm, low-stress SiN_x layer is grown by low-pressure chemical vapor deposition, LPCVD. The bottom SiN_x layer is patterned by photolithography and then etched by reactive ion etching

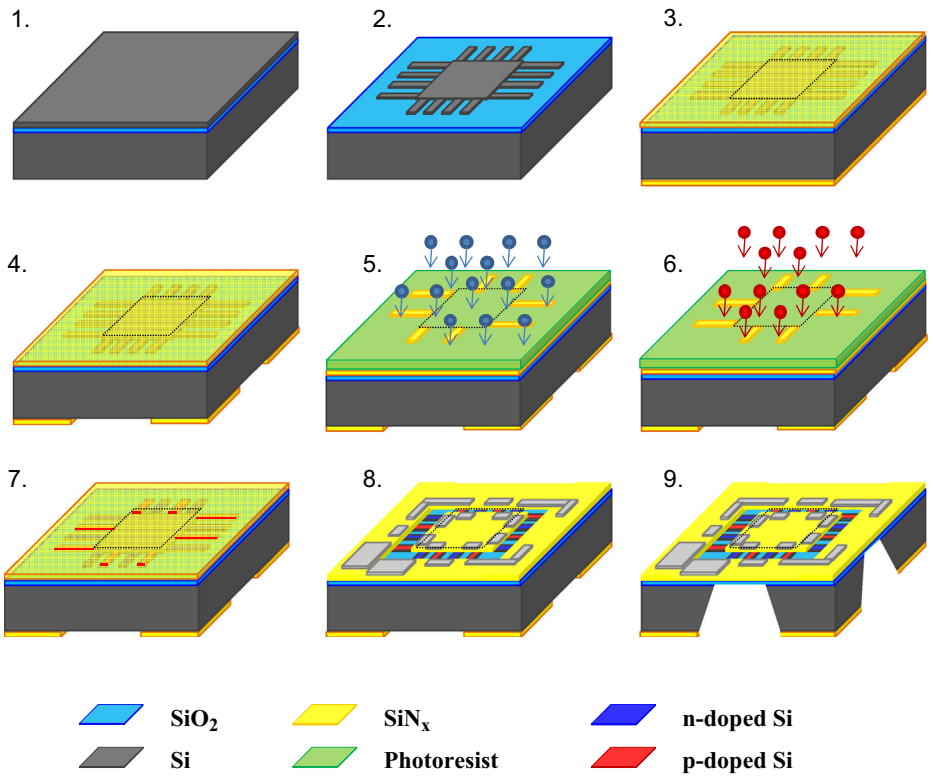

Figure 2 Sketch of the main microfabrications steps: 1. Thinning of the Si layer. 2. Patterning of the Si membrane. 3. Growth of SiN_x. 4. RIE in the backside to open window. 5 and 6. n, p implantation. 7. Post annealing to activate dopants. 8. Photolithography to define metal lines and contacts. 9. Backside Si bulk etching.

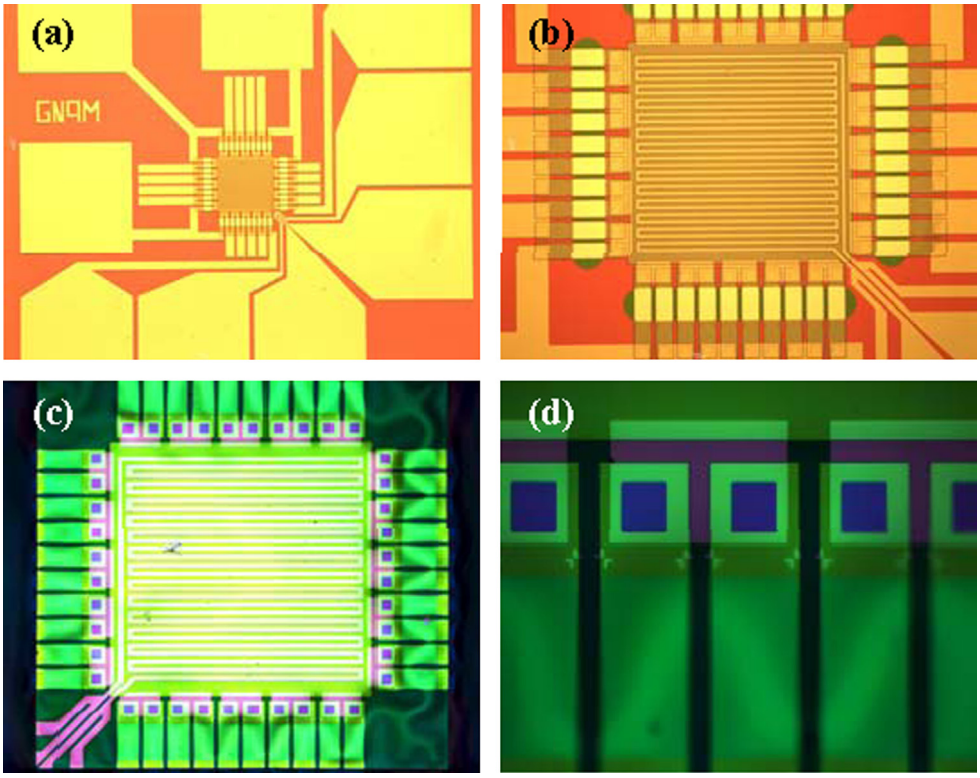

Figure 3 Optical microscope images of a fabricated device before opening the back side (a, b) and after (c, d). Figure d shows a detailed view of the n, p regions and the open vias used for contacts.

(RIE), leaving windows to facilitate the removal of the Si wafer in the last step. The n, p regions are defined by using a photoresist mask, followed by sequential implantation of Boron and Phosphorous and Rapid Thermal Annealing (RTA) at 900 °C. Details of this step will be covered in the next section. After dopant activation, vias are opened at the edges of the doped regions to permit contacts with the metal and also in the middle of the n, p regions to decrease the thermal link between the Si frame and the suspended membrane. Figure 3 shows optical microscope images of the final device where it is possible to appreciate the implanted regions and open via contacts. Ni, 50 nm thick, is grown by sputtering, followed by thermal treatment at 300 °C to form NiSi and achieve ohmic contacts with the doped Si regions. The final step consists of a wet etching of the back side to leave the central Si platform suspended. In this prototype, this step has been performed by using KOH attack but CMOS compatible procedures like tetramethylammonium hydroxide (TMAH) can also be used.

n and p-type doping of ultrathin Si layers

Ion implantation followed by rapid thermal annealing to recrystallize the amorphized material and activate dopants is the standard procedure to increase carrier concentration in semiconductors. Although the microscopic processes behind an effective doping are complex, very well established recipes exist for bulk Si. However, unlike their bulk counterpart, doping ultrathin layers requires additional strategies to achieve the adequate carrier concentration without compromising the structural stability of the film. Since the high mobility of the carriers depends on the crystalline quality of the material, epitaxial recrystallization must be ensured by appropriate post-processing annealings. A single-crystalline layer, free of defects, acting as a seed for epitaxial ordering of the damaged region during rapid thermal processing, is thus required at the bottom part of the implanted layer. We use the SRIM software package to determine the doses and energies required to achieve the desired carrier concentration, and guarantee a low-damaged region at the bottom of the Si layer. The temperature of the rapid thermal processing is another key aspect in impurity activation when dealing with very thin layers of Si on SiO_2. Temperatures above 950 °C will rupture the film by dewetting due to the surface tension between crystalline Si and SiO_2 [16,17]. As the best compromise to facilitate activation and avoid structural damaging of the layer we have adopted a RTA procedure with $T=900$ °C.

Finite element modeling

3D modeling of the output power for different temperature loads is realized by the COMSOL Multiphysics simulation package, which allows the solution of common arbitrary partial differential equations (PDEs) of a field variable on a given volume. Finite Element Modeling, FEM, was carried out with the cold region at room temperature and the materials parameters listed in Table 1. The main results are shown in Figure 4. Figure 4 shows the voltage output (a) and

Table 1 Material properties, thermal conductivity κ, electrical resistivity ρ, and Seebeck coefficient S, used in the Multiphysics modeling of the TEG.

Material	k [W/mK]	ρ [Ω cm]	S (V/K)
SiO_2	1.4	10^{16}	
SiN_x	3	1000	
Ni	93	6.24×10^{-8}	-15×10^{-6}
Si (central region)	150	14-22	0
Si (doped legs)	60	1×10^{-2}	4.0×10^{-4}

Contact resistance Ni/NiSi/Si=1.7×10^{-6} Ω cm^{2}.

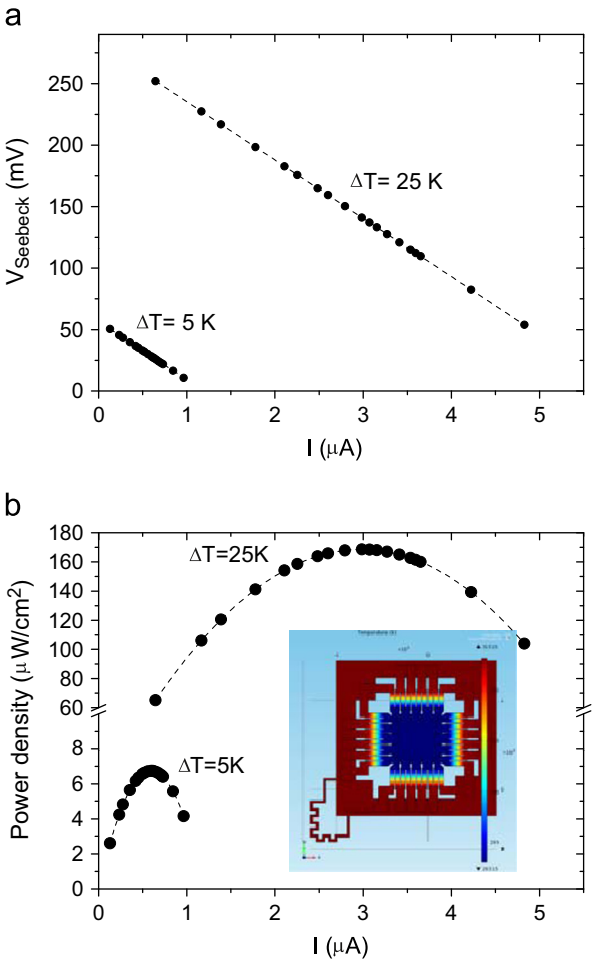

Figure 4 Finite Element Modeling of the thermoelectric microgenerator. Output voltage (a) and power density (b) as a function of current for two temperature differences across the structure. The inset in figure b shows the 2D map use for the simulations.

the output power density (b) as a function of current, measured by varying the R_{load}. Maximum power densities of 6.7 and 168 μW/cm^2 are attained at $R_{load}=R_{int}$ for $\Delta T=5$ and 25 K, respectively. The inset of Figure 4b shows the 2D temperature contour in the device. The structure yields a Seebeck voltage at open circuit of 285 μV/K, which reflects that S is dominated by the n and p-type doped Si regions embedded in the Si membrane.

Experimental results on TEG behavior

The experimental conditions to achieve a good contact resistance between Ni and n and p-type doped Si were evaluated by using specific test structures to determine the contact resistance. As briefly mentioned in section 2.1, after Ni growth, the devices were annealed at 300 °C to form NiSi. This procedure reduced the interfacial contact resistance to values around 1.7 μΩ cm^{-2}. The resistance of the Si layer and the mobility of the carriers were evaluated with a Hall setup. In the n-type material for a doping level of 2×10^{19} cm^{-3},we measured a mobility of 80 cm^2/Vs, and for p-type Si with a doping of 6.5×10^{18} cm^{-3}, we obtained $\mu=50$ cm^2/Vs. Those values are compatible with bulk Si [18] and corroborate an epitaxial regrowth of the thin Si layer in the conditions stated above. The internal resistance of a single device with 20 np regions connected electrically in series is about 40 kΩ. This value closely agrees with the calculated one, 38 kΩ, based on the dimensions of the material and the electrical resistivity of both n and p-type regions.

Thermoelectric characterization

We impose a temperature gradient between the hot and cold regions of the device by contacting the Si frame to a hot plate, that served as a heat-source in harvesting configuration, while cooling the central part of the chip (suspended Si membrane) by convective cooling with a fan (Figure 5a). In steady-state the temperatures of the central and outside regions of the device are measured by means of two metal resistances located at both sides. The Seebeck voltage at open circuit was quantified under various temperature differences across the structure ranging from 1 to 5.5 K. The length of the active region of the device is 150 μm. The results for the 100 nm thin Si membrane are shown in Figure 5b-d. The measured Seebeck coefficient, obtained from the slope of the open circuit voltage versus the temperature difference (Figure 5b), is 354 μV/K per a unileg (7.1 mV across a 10 np legs device). Previous studies have shown that the Seebeck coefficient of SOI wafers with Si thicknesses above 6 nm is similar to bulk Si [19]. As the Seebeck coefficient of the structure is largely dominated by the n, p Si regions, we infer an average doping level of $\sim 10^{19}$ cm^{-3}, that roughly matches our estimations from the test structures. Since, in a 100 nm thick single-crystalline layer the electrical resistivity is also analogous to bulk Si, the main impact of reduced thickness of the Si membrane on the figure of merit is the decrease of thermal conductivity by approximately 3-fold compared to bulk Si [20]. This basically means that the device is able to withstand higher temperature differences under the same applied temperature loads compared to previous devices that used much thicker films of poly-Si [7,8]. Further reduction of the Si thickness will diminish the thermal conductivity even further at the expense of an increase of the internal resistance which may require complex signal conditioning steps to power output devices.

The thermoelectric characterization of the microdevice is accomplished by using a load resistor connected in series with the TE generator. *I-V* curves are obtained by changing the value of the load resistor. The results for various temperature differences are shown in Figure 5b and c. As expected and shown above in Figure 4 from the modeling

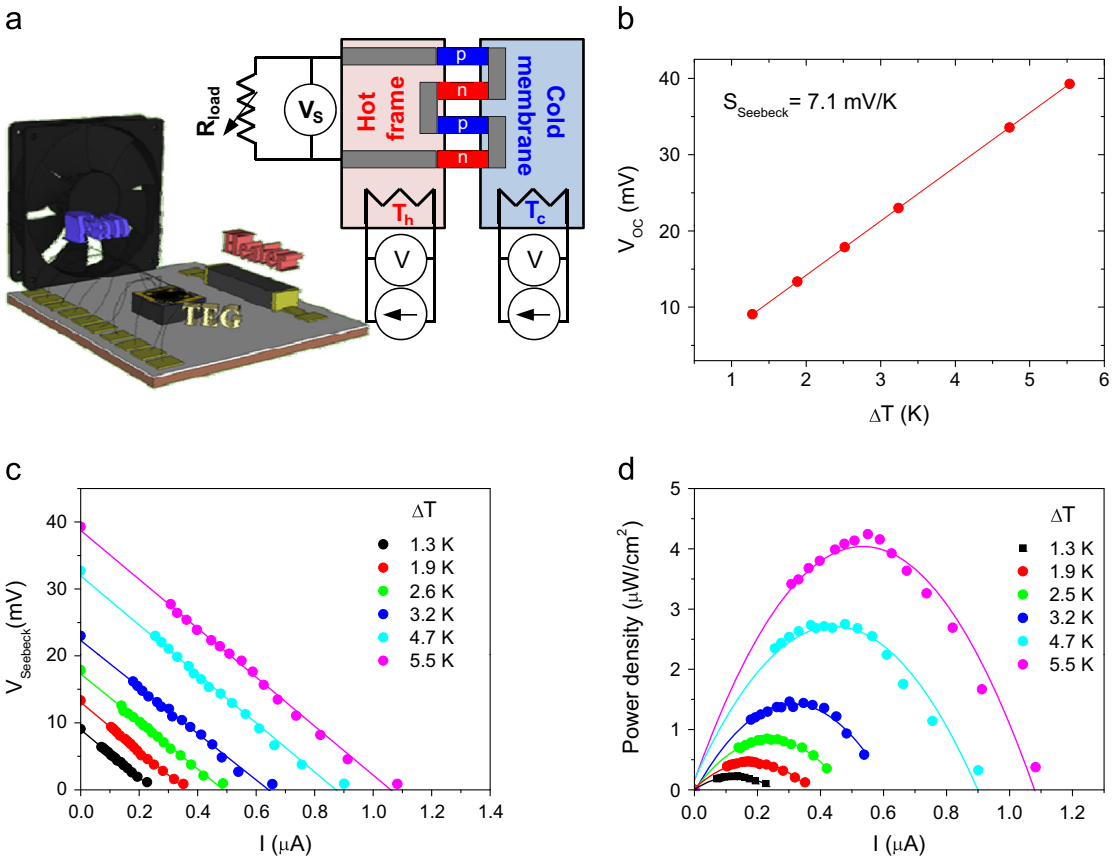

Figure 5 (a) Schematic design of the experimental setup to measure thermoelectric behavior. (b) Voltage at open circuit as a function of the temperature difference Measured voltage (c) and power generation per unit area (d) versus current for the TEG device. Different values of temperature difference were used for each series as shown in the legend.

of the thermoelectric response, the maximum power output occurs at R_{load}-R_{int}. From the measured data a power output of 4.5 μW/cm^2 under a temperature difference of 5.5 K is obtained, which is comparable to the value obtained from Finite Element Modeling of the structure. This value compares well to previously reported Si-based micro/nanogenerators [12-14,21]. Considering that the maximum power output increases parabolically with ΔT, $P \alpha \Delta T^2$ [1], the power output achieved with our device at ΔT=5 K is higher than those found in other planar Si-based thermo generators, such as the one based on Si-Al thermopiles [7] or on bottom-up Si NWs [14]. In future, further device optimization, reducing the Si thickness and simultaneously improving chip design will certainly result in improved power outputs and thermal gradients across the structure. Improved design should maximize the parallel configuration of the n,p regions to reduce the internal resistance. Thermal coupling of the central membrane to a heat sink and encapsulation of the device are also important considerations for practical applications. Under optimum conditions the microgenerator could ultimately be used as an energy harvester to power small devices such as mobile and wireless electronics. For sensing applications requiring discontinuous monitorization, the proposed device can be integrated into wearable thermoelectrics for body scavenging purposes or into higher temperature sources such as exhaust hot pipes. A back-of-the-envelope calculation shows that a 10 cm^2 TEG device could provide power outputs around 50 μW during energy body scavenging in appropriate ambient conditions. Collecting energy for about 2 min would provide about 6 mJ, which is enough to run a low power device such as a heart rate monitor.

Conclusions

We have fabricated a first prototype of a CMOS compatible planar microthermoelectric generator that contains ultrathin Si membranes as the active TE material and therefore can be integrated into standard Si chips. A power output of 4.5 μW/cm^2 was achieved under a temperature difference of 5.5 K. Patterning the membrane into Si nanowires or reducing its thickness to few nm could result in substantial improvements by reducing the thermal conductivity of the structure. In addition, the proposed design permits the fabrication of multiple optimized generators on a single wafer to be connected in series to boost the voltage performance or in parallel to increase current output to match the desired application.

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